Investor Presentation

November 2021

Safe Harbor

This presentation contains forward-looking statements concerning Atomera Incorporated (““Atomera,” the “Company,” “we,” “us,” and “our”). The words “believe,” “may,” “will,” “potentially,” “estimate,” “continue,” “anticipate,” “intend,” “could,” “would,” “project,” “plan,” “expect” and similar expressions that convey uncertainty of future events or outcomes are intended to identify forward-looking statements. These forward-looking statements are subject to a number of risks, uncertainties and assumptions, including those disclosed in the section "Risk Factors" included in our Annual Report on Form 10-K filed with the SEC on February 19, 2021. In light of these risks, uncertainties and assumptions, the forward-looking events and circumstances discussed in this presentation may not occur and actual results could differ materially and adversely from those anticipated or implied in our forward-looking statements. You should not rely upon forward-looking statements as predictions of future events. Although we believe that the expectations reflected in our forward-looking statements are reasonable, we cannot guarantee that the future results, levels of activity, performance or events and circumstances described in the forward-looking statements will be achieved or occur.

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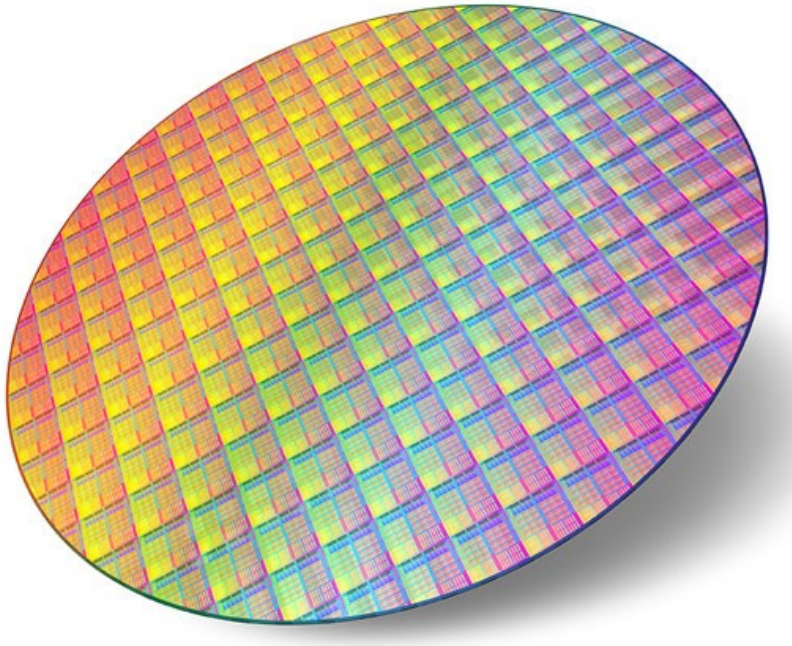
Investment Overview

- **Mears Silicon Technology (MST®) is a thin film used to enhance semiconductors**
  - Results in higher performance, lower power, and lower costs for ICs
- **Capital-light IP and technology licensing business**
  - Robust and growing patent portfolio
- **Engaged with 50% of world's top semiconductor makers**
- **Licenses with four companies including recent JDA**
- **Strong team to commercialize technology**



A Better Way for Industry R&D

Industry Consortia

Little Control

Expensive & Inefficient

Equipment OEMs

No Longer Available

Tied to Equipment Sales

In House R&D

Large Scale, Long Term Investment

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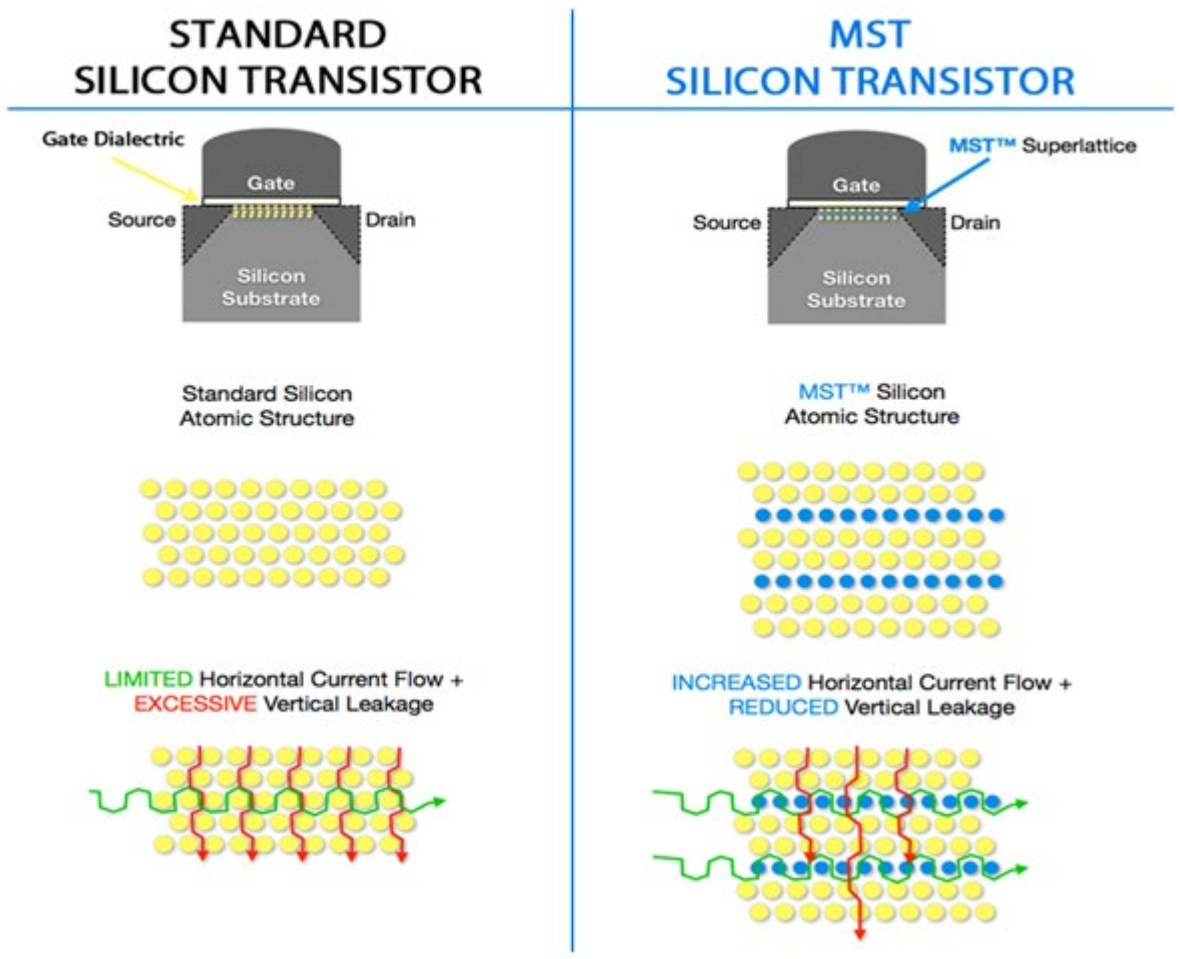
Targeted Innovation

Inexpensive & Low Risk

MST Technology

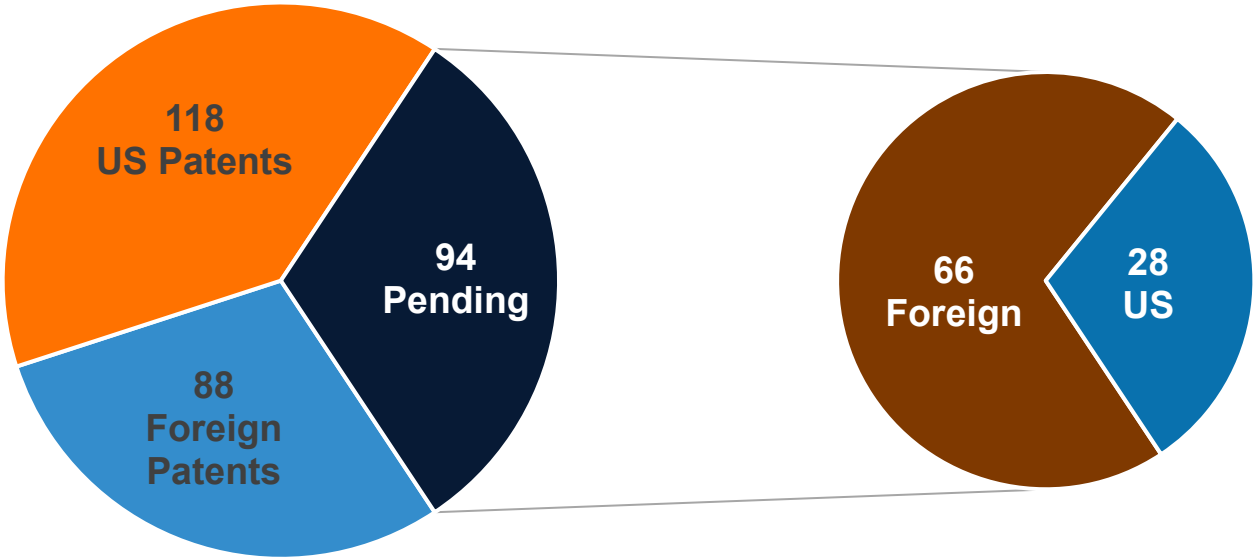


Potential Benefits

- **Improved Efficiency**
  - Higher transistor performance
  - Lower power consumption
  - Better reliability
- **Lower cost**
  - Reduced die size
  - Improved yield
  - Higher throughput
- **Same benefits as a node shrink**

IP Portfolio Grew >20% YoY

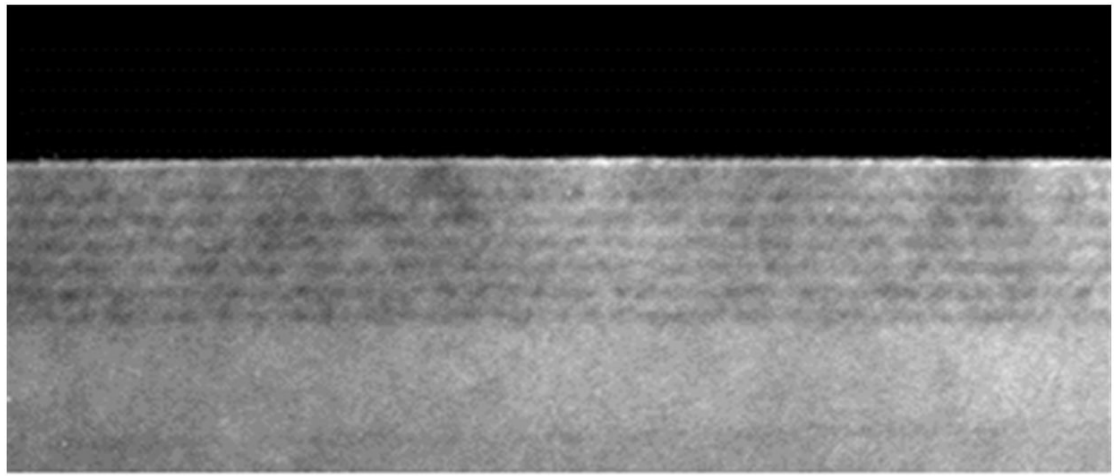
300 Patents Issued and Pending



Core MST Method and Device
MST Enabled Devices/Architecture
Next-Gen Architectures using MST

Discoverable

These distinctive layers are visible on products using MST



Extensive know-how

Extends life and value of patents

Target Customers & Partners

Integrated Device Manufacturers

SAMSUNG · Micron · TOSHIBA · intel

Texas Instruments · ST · Infineon · ON

RENESAS · NXP · AsahiKASEI · SK hynix

Foundry

tsmc · GLOBAL FOUNDRIES · UMC · SMIC

HHGrace · DB HiTek · TOWERJAZZ · MagnaChip

Fabless

BROADCOM · MARVELL · maxim integrated · MICROCHIP

SKYWORKS · QUALCOMM · XILINX · qorvo

Tool Suppliers (Partners)

ASM · APPLIED MATERIALS · KOKUSAI SEMICONDUCTOR EQUIPMENT CORPORATION · SYNOPSYS

Customer Engagement & Revenue Model

		Customer Wafer Manufacturing				
		Atomera MST® Deposition		Customer MST® Deposition		
Phase	**1**. Planning	**2**. Setup	**3**. Integration	**4**. Installation	**5**. Qualification	**6**. Production

Engineering Service Fees

- MST deposition on customer wafers
- Integration consulting

License Fees

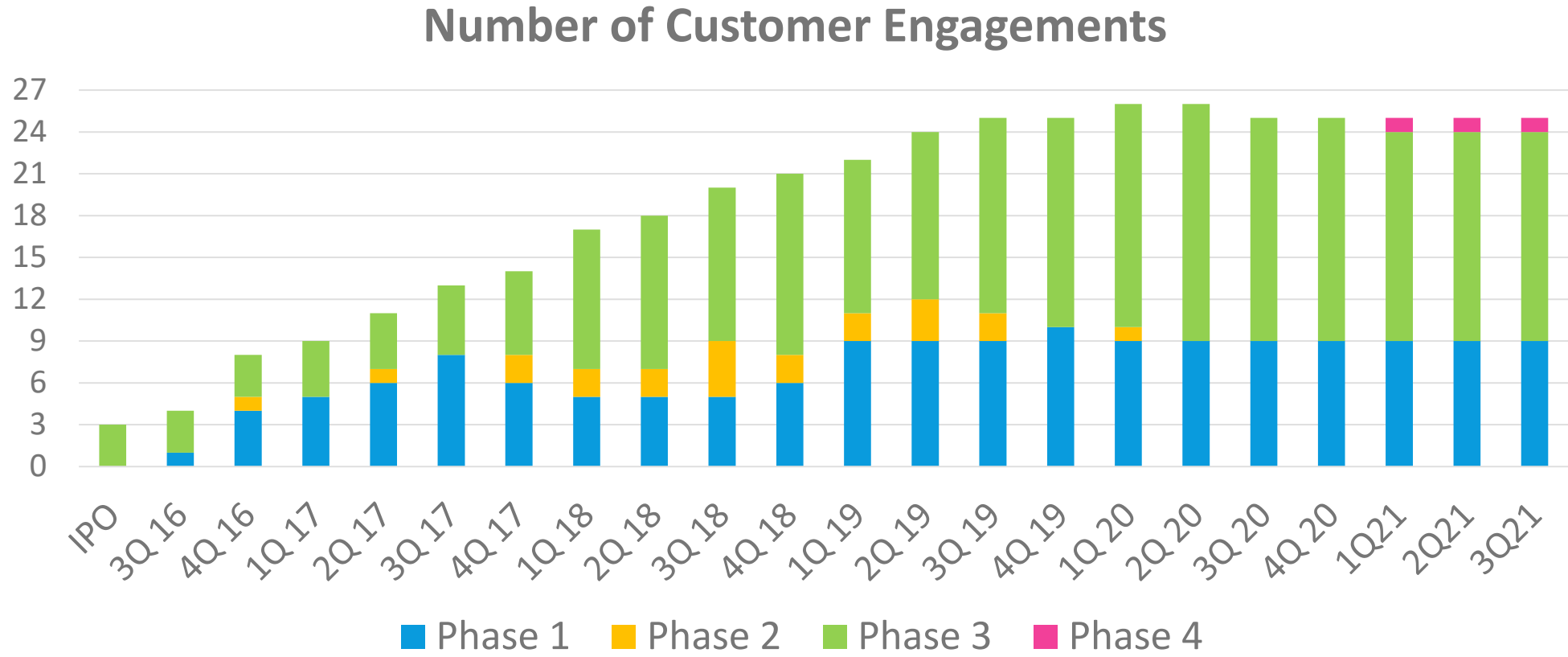
- Integration licenses
- Manufacturing licenses
- Distribution licenses

Joint Development Agreements

Royalties

Customer Engagement Model

Customer Pipeline



- 19 customers, 25 engagements
- Working with 50% of the world's top semiconductor makers*

* At least 10 of the top 20 (IC Insights, McClean Report 2021)

Royalty Opportunity

- **~370 wafer fabs operating worldwide**
- **Adoption of MST in one fab can make Atomera profitable from royalties alone**
  - 2021 non-GAAP OPEX guidance is $14.00-14.5M

Example 1 | Worldwide Average Fab	
Monthly Fab Capacity[1] *(wafers/month)*	49,000
Industry average wafer ASP - 2018	$1,136
Annual Revenue Potential[2]	**$13M**
Annual Revenue at 50% of ramp[2]	$6.7M

Example 2 | Leading Foundry, 28nm Fab	
Monthly Fab Capacity *(wafers/month)*	80,000
Industry average 28nm wafer ASP	$3,000
Annual Revenue Potential[2]	**$58M**
Annual Revenue at 50% of ramp[2]	$29M

1. Represents wafers starts per month (200mm equiv) – 217.3M starts in 370 fabs
2. Assumes 2% royalty rate

Source: IC Insights Global Wafer Capacity 2019-2023 report, McClean Report 2019

MST Customer Business Opportunity

Standard industry fab wafer pricing, GM, and cost

	Price	GM%	GM$ Increase	MST Royalty	Cost	
28nm HP wafer	$ 3,000	45%	$ -	$ -	$ 1,650	
28nm HP+ wafer	$ 3,150					$150 price increase for +15% performance

Fab gets a 30% performance improvement or 25% shrink via MST

MST processing cost					$ 20	Incremental cost of depositing MST
28nm HP wafer with MST	$ 3,300	47.4%	$ 214	$ 66	$ 1,736	$300 price increase for +30% performance
28nm HP wafer with MST	$ 3,375	48.5%	$ 288	$ 68	$ 1,738	12.5% price increase for 25% size reduction

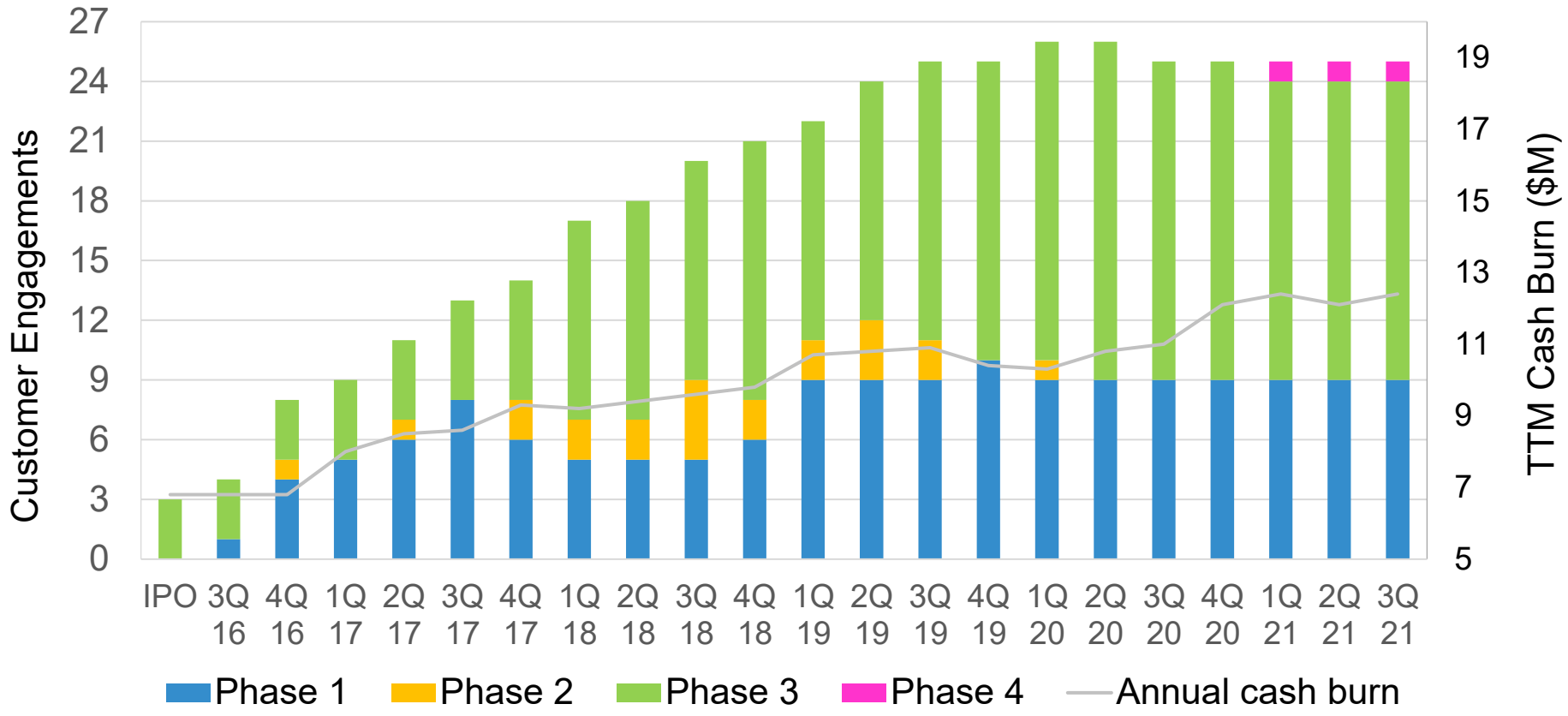
Fabless customer benefit in die shrink case

	Chip sales/ wafer*	GM%	GM$ Increase	Product ASP	Die/wafer	
28nm HP wafer	$ 8,400	50.0%	$ -	$ 4.42	2,235	Baseline business for 30mm^2 chip
28nm HP wafer with MST	$ 11,279	62.8%	$ 2,879	$ 4.42	3,001	Improved financials with 25% size reduction

Everyone in the value chain benefits from MST technology

* Yielded

Cash Efficient Growth



Financial Review

	Q3 '20	Q4 '20	Q1 '21	Q2 '21	Q3 '21
GAAP Results					
Revenue	$ -	$ -	**$0.4M**	$ -	$ -
Gross Profit	$ -	$ -	$0.4M	$ -	$ -
Operating Expense					
R&D	$2.0M	$2.2M	$2.2M	$2.1M	$2.3M
G&A	$1.3M	$1.4M	$1.5	$1.5M	$1.6M
S&M	$0.2M	$0.3M	$0.3M	$0.1M	$0.3M
Total Operating Expense	**$3.6M**	**$3.9M**	**$4.0M**	**$3.7M**	**$4.1M**
Net Loss	($3.6M)	($3.9M)	($3.6M)	($3.7M)	($4.2M)
Loss Per Share	*($0.19)*	*($0.19)*	*($0.16)*	*($0.17)*	*($0.19)*
Reconciliation between GAAP & Non-GAAP					
Net Loss (GAAP)	**($3.6M)**	**($3.9M)**	**($3.6M)**	**($3.7M)**	**($4.2M)**
Stock-Based Compensation	$0.8M	$0.8M	$0.7M	$0.8M	$0.8M
Other income (expense)*	-	-	-	-	$0.1M
Adjusted EBITDA (Non-GAAP)**	**($2.7M)**	**($3.0M)**	**($2.9M)**	**($2.9M)**	**($3.4M)**

Balance Sheet 9/30/21	
Cash	**$31.8M**
Debt	**-**
Shares Outstanding	**23.1M**

Some figures may not total exactly due to rounding

**Includes depreciation, interest income/expense and provision for income tax*

***Adjusted EBITDA is a non-GAAP financial measure. A full reconciliation of GAAP and non-GAAP results is contained in our Q3 press release.*

Summary

- High margin, recurring revenue financial model
- Strong technology, patent position, and balance sheet
- Traction with many top industry players and growing licensee base
- Ramping commercial license revenues

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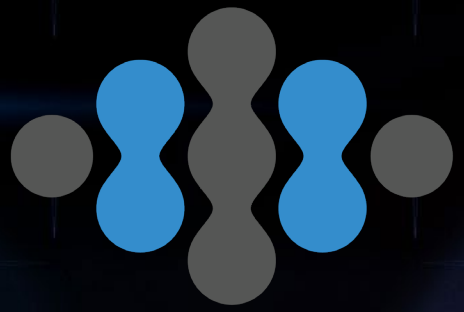
Thank You



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Backup Slides

Customer Engagement Model

Standard customer engagement

		Customer Wafer Manufacturing				
		Atomera MST® Deposition		Customer MST® Deposition		
Phase	Planning	Setup	Integration	Installation	Qualification	Production

Joint development engagement

		Atomera MST® Deposition		Customer MST® Deposition		
Phase	Planning	Setup	Integration	Installation & Integration	Qualification	Production

MST technology focus areas

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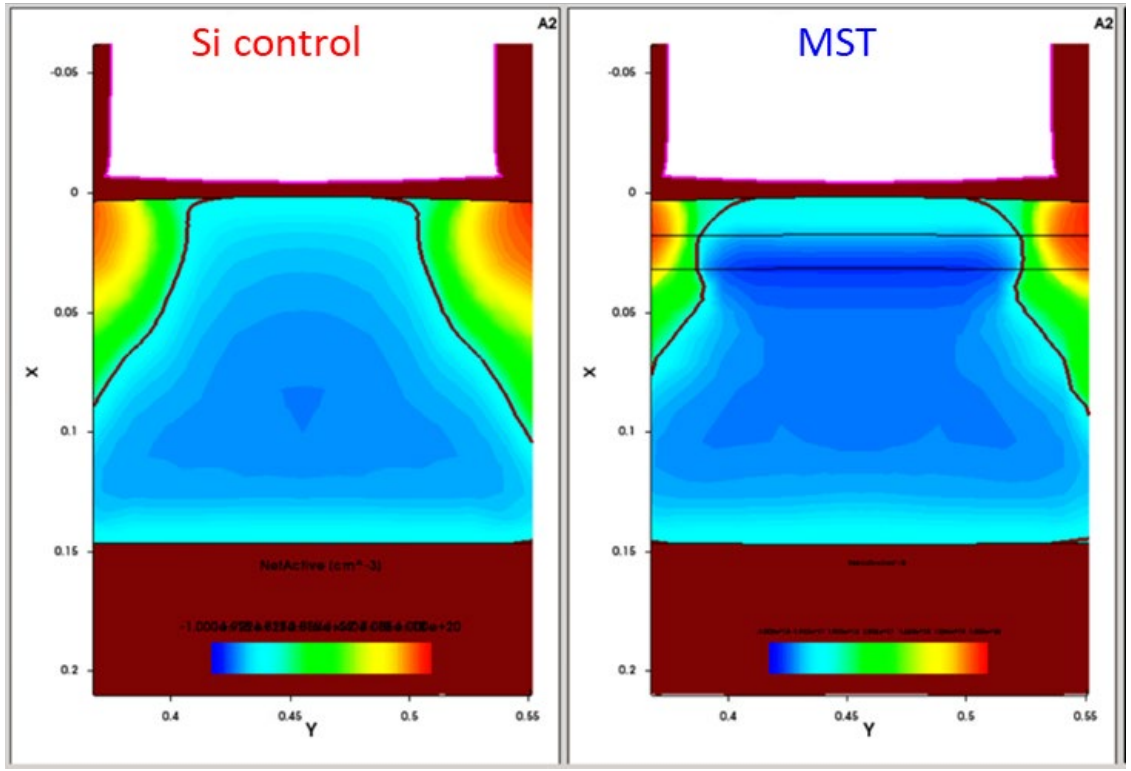
MST-SP

MST for RF-SOI

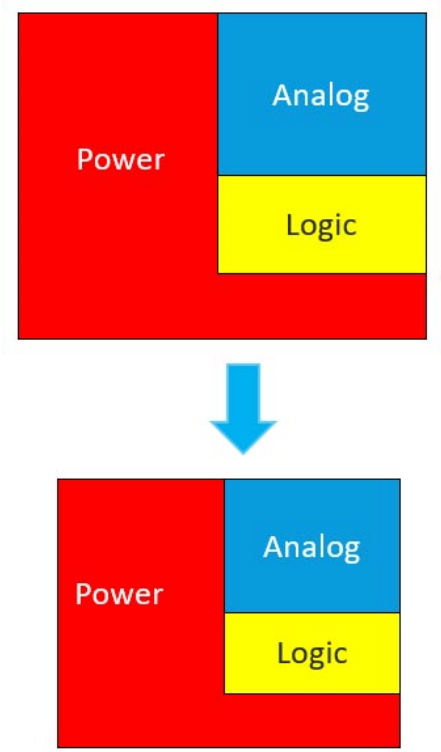
MST for Advanced Nodes

Atomera MSTcad™

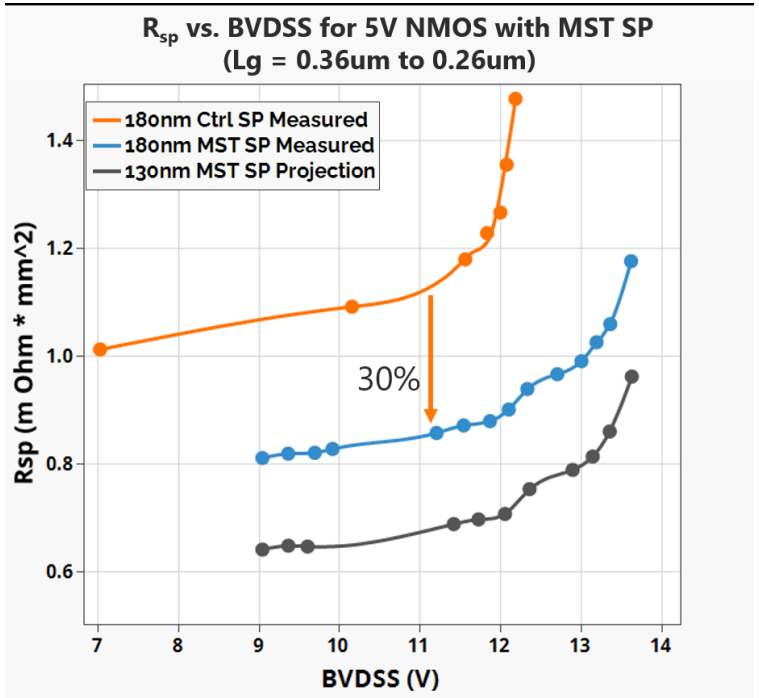
- **Leading semiconductor companies use TCAD to model manufacturing processes**
  - MSTcad is an add-on for MST
- **MSTcad can speeds up the time needed to evaluate multiple MST integration options**
- **Lowers cost of MST evaluation**
- **Speeds time to successful wafer runs**
- **Fewer wafer runs lead to faster production**



MST enables legacy capacity expansion

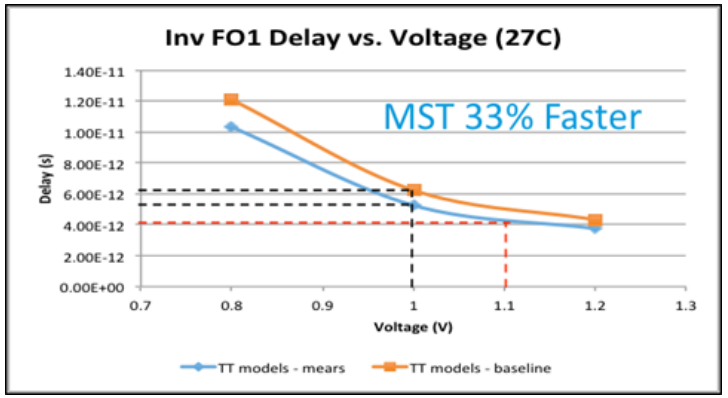


- **MST provides 30% performance advantage**
  - 0.13u analog design
  - MST vs control silicon
- **Enables a die shrink of 15-20%**
- **Smaller die means more manufacturing capacity**
  - Without the cost of building a new fab



MST 28nm benefits

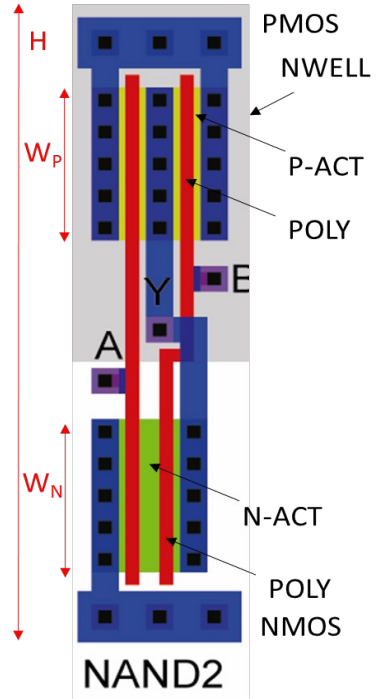
MST shows 30% higher performance



MST performance improvement due to:

- Higher electron mobility
- Improved gate oxide integrity enabling higher overdrive

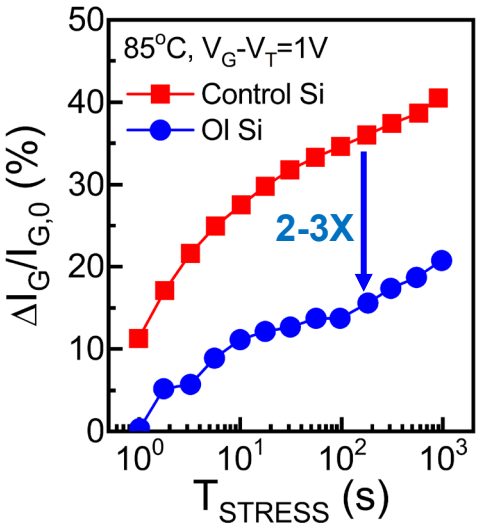
- **Performance improvements due to MST can be traded for area reduction**
- **28nm PDK SPICE model used to showcase:**
  - Logic scaling with MST shows 22-25% area reduction
    - Using a NAND2 gate
  - Analog scaling with MST shows up to 21% area reduction
- **Implementation of MST on new 28nm designs can result in >20% more production capacity**
- **Allows excellent economic benefits for the whole value chain**



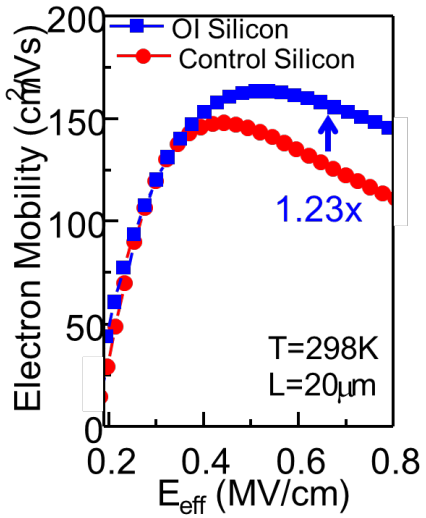
MST for High-k metal gate (HKMG) transistors

- **MST enhances HKMG transistor performance and reliability***
  - Reduced stress induced leakage current (SILC) enabling reliability improvement
  - 23% long-channel mobility enhancement
  - 2.7x lower gate leakage

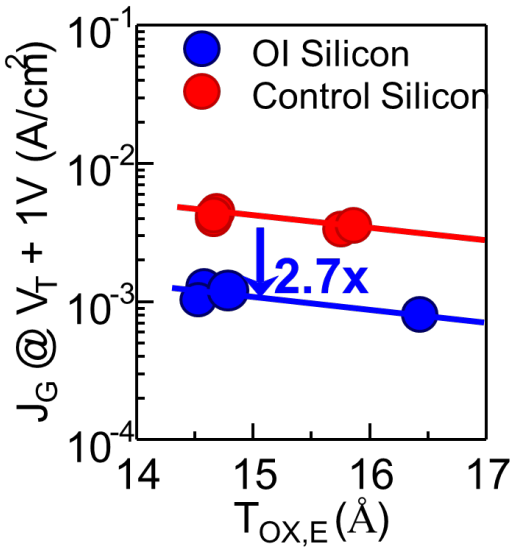
SILC



e⁻ mobility



J_G vs. *EOT*



* Professor Suman Datta Group

UNIVERSITY OF NOTRE DAME

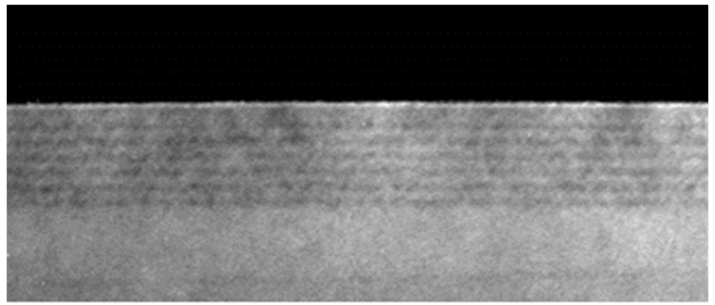
Joint Development Agreements

- Advantages of joint development
  - Atomera and customer engineers aligned on common goal
  - Customer “resident expert” team develops expertise on Atomera technology
  - Resident experts become natural advocates
- First JDA signed with market leading semiconductor company
  - Includes a manufacturing license, putting them in Phase 4
  - Upon completion, MST can more easily be adopted by business units
  - Each business unit is an incremental licensing opportunity

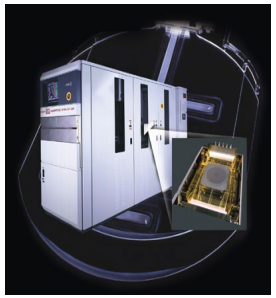
MST: Mears Silicon Technology

Quantum Engineered Silicon

Partial Monolayers of Oxygen in Silicon

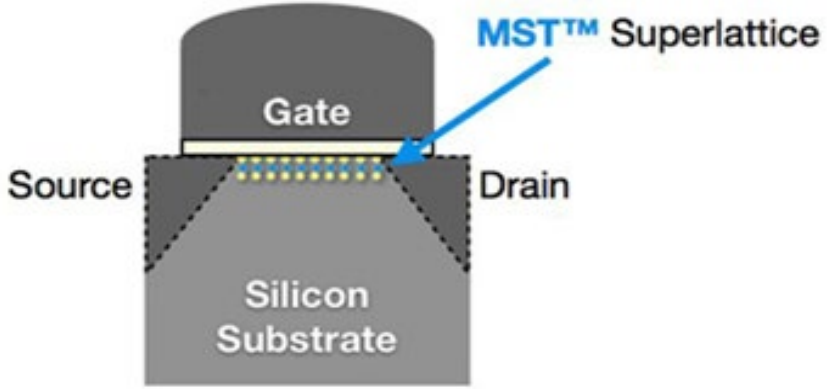


Supported by Major Semiconductor Tool Suppliers

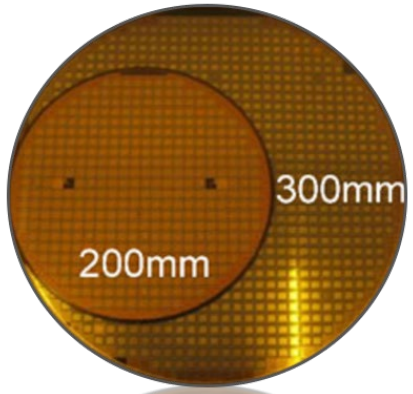


ASM KOKUSAI SEMICONDUCTOR EQUIPMENT CORPORATION APPLIED MATERIALS

MST Enhanced Transistors



Atomera state of the art research center



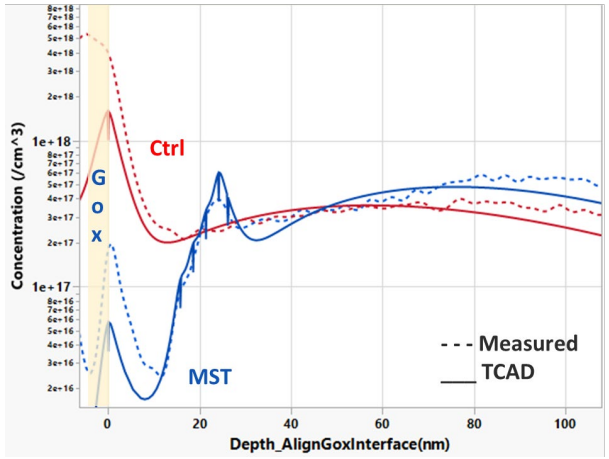
Epi Deposition Tool

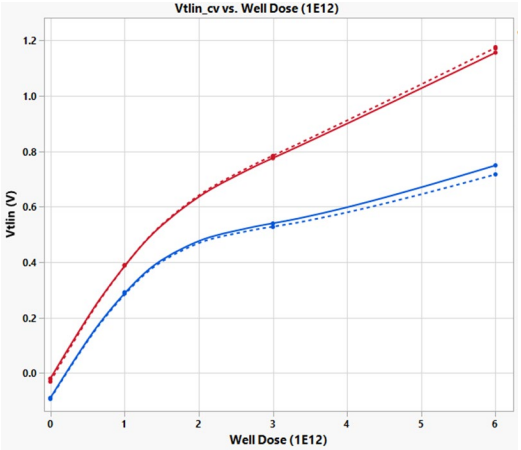
- **Epi deposition facility**
  - 300mm Epi deposition
  - 200mm Epi deposition
  - Wafer cleaning equipment
  - Metrology tools
  - Advanced wafer handling
  - World class clean room facility
- **Available to deliver customer wafers**

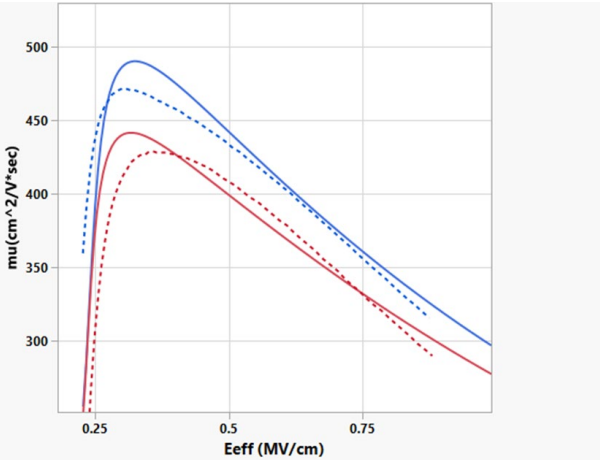
Atomera MSTcad™ Progress

- Leading semiconductor companies use TCAD
- MST is modelled with a TCAD add-on called MSTcad
- These plots show silicon verification of MSTcad simulations
- Enables good electrical match-up for 5V NMOS and MST SP
- Should speed time to successful results with customers

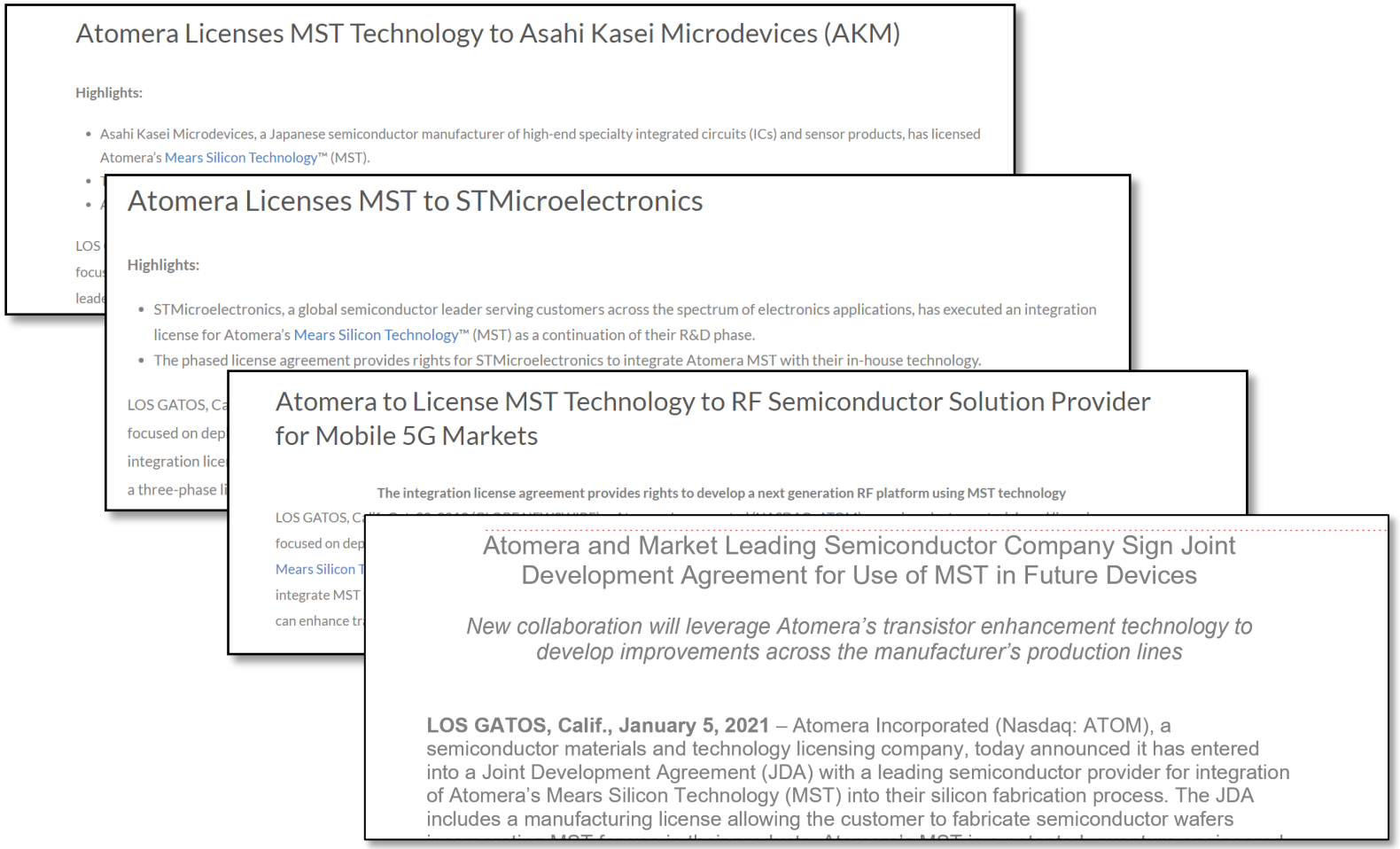
Boron 6E12 15KeV SIMS







Atomera Licensees



Atomera Licenses MST Technology to Asahi Kasei Microdevices (AKM)

Highlights:

- Asahi Kasei Microdevices, a Japanese semiconductor manufacturer of high-end specialty integrated circuits (ICs) and sensor products, has licensed Atomera's Mears Silicon Technology™ (MST).

Atomera Licenses MST to STMicroelectronics

Highlights:

- STMicroelectronics, a global semiconductor leader serving customers across the spectrum of electronics applications, has executed an integration license for Atomera's Mears Silicon Technology™ (MST) as a continuation of their R&D phase.
- The phased license agreement provides rights for STMicroelectronics to integrate Atomera MST with their in-house technology.

Atomera to License MST Technology to RF Semiconductor Solution Provider for Mobile 5G Markets

The integration license agreement provides rights to develop a next generation RF platform using MST technology

Atomera and Market Leading Semiconductor Company Sign Joint Development Agreement for Use of MST in Future Devices

New collaboration will leverage Atomera's transistor enhancement technology to develop improvements across the manufacturer's production lines

LOS GATOS, Calif., January 5, 2021 – Atomera Incorporated (Nasdaq: ATOM), a semiconductor materials and technology licensing company, today announced it has entered into a Joint Development Agreement (JDA) with a leading semiconductor provider for integration of Atomera's Mears Silicon Technology (MST) into their silicon fabrication process. The JDA includes a manufacturing license allowing the customer to fabricate semiconductor wafers

AsahiKASEI

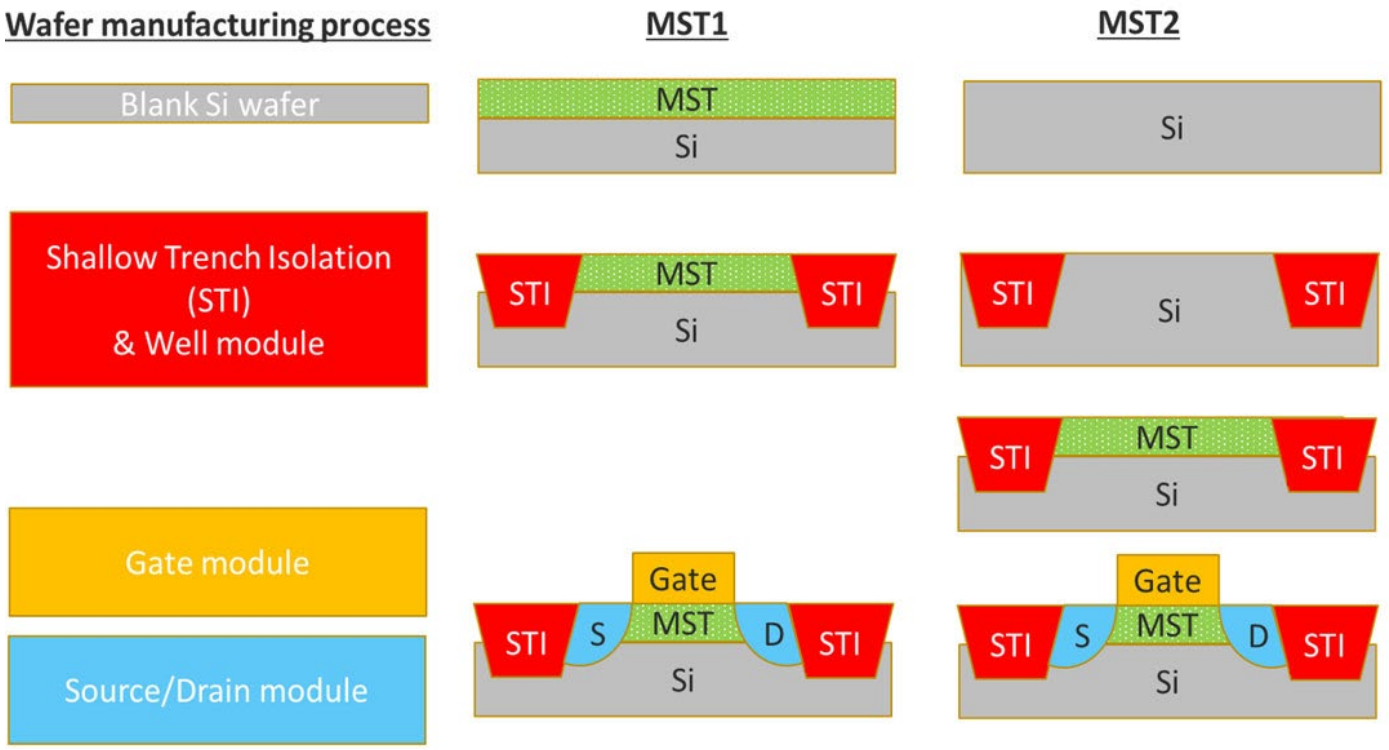
life.augmented

Large fabless RF semiconductor company

Market Leading semiconductor company

MST1 vs MST2

- **MST1**
  - Blanket technology
  - Easy to integrate
  - Deposited at beginning of mfg process
  - Degraded by high heat in STI/Well module
  - Faster time to market for low heat processes
  - Used for FinFET, RFSOI, newer process nodes
- **MST2**
  - Selective technology
    - Integrated after STI/Well so avoids highest heat
  - More flexible to apply to selected areas only
  - Used for 5V, Analog, older process nodes



MST Matching Performance

- **Transistor mismatch is an industry problem**
- **Certain circuit designs benefit from mismatch reduction**
  - A-D convertors
  - SRAM
  - Flash
  - DRAM sense amplifiers
- **MST can reduce mismatch by more than 50%**
- **Details available at Atomera's website**
  - blog.atomera.com